CLAIMS

We claim:

1. A method of adaptively electropolishing a metal layer formed on a semiconductor wafer, the method comprising:

electropolishing a portion of the metal layer, wherein portions of the metal layer are electropolished separately;

before electropolishing the portion, determining a thickness measurement of the portion of the metal layer to be electropolished; and

adjusting an amount that the portion is to be electropolished based on the thickness measurement.

2. The method of claim 1, wherein electropolishing a portion of the metal layer comprises:

applying a stream of electrolyte to the portion of the metal layer through a nozzle adjacent to the portion of the metal layer.

3. The method of claim 2, wherein the wafer is held, rotated, and translated using a wafer chuck while the nozzle is held stationary adjacent to the metal layer.

4. The method of claim 2, wherein the wafer is held and rotated using a wafer chuck while the nozzle is translated adjacent to the metal layer.

5. The method of claim 2, wherein adjusting an amount that the portion is to be electropolished comprises:

adjusting a polishing current or voltage applied to the stream of electrolyte.

6. The method of claim 2, wherein adjusting an amount that the portion is to be electropolished comprises:

adjusting a polishing duration of the portion.

7. The method of claim 1, wherein determining a thickness measurement comprises:

obtaining a map of the thickness measurement of the metal layer determined using a thickness metrology tool.

8. The method of claim 7, wherein determining a thickness measurement further comprises:

measuring thickness measurements of the metal layer using an end-point detector; and

wherein adjusting an amount that the portion is to be electropolished comprises:

adjusting the amount that the portion is to be electropolished during an initial polishing using the map of the thickness measurement of the metal layer determined using the thickness metrology tool; and

adjusting the amount that the portion is to be electropolished during a subsequent polishing using the thickness measurement measured using the end point detector.

9. The method of claim 7, further comprising:

interpolating a thickness measurement of a portion of the metal layer not having a thickness measurement on the map based on a plurality of thickness measurements of portions of the metal layer having thickness measurements on the map.

10. The method of claim 1, wherein determining a thickness measurement comprises:

measuring thickness measurements of the metal layer using an end point detector adjacent to the metal layer.

11. The method of claim 10, wherein the wafer is held, rotated, and translated using a wafer chuck while the end point detector is held stationary adjacent to the metal layer.

12. The method of claim 10, wherein the thickness measurements are mapped using a plurality of pixel partitions, wherein a pixel position corresponds to a field that can be measured using the end point detector.

13. The method of claim 10, further comprising:

determining an end to polishing the portion based on a metal density of pattern on the wafer.

14. The method of claim 10, wherein the end point detector is an optical sensor.

15. The method of claim 10, wherein the end point detector is an eddy current sensor.

16. A system for adaptively electropolishing a metal layer formed on a semiconductor wafer, the method comprising:

an electropolishing module configured to electropolish portions of the metal layer separately; and

a control system configured to:

determine a thickness measurement of a portion of the metal layer before the portion is electropolished, and

adjust an amount that the portion is electropolished based on the thickness measurement.

17. The system of claim 16, wherein the electropolishing module comprises:

a nozzle configured to apply a stream of electrolyte to the portion of the metal layer.

18. The system of claim 17, further comprising:

a wafer chuck configured to hold, rotate, and translate the wafer while the nozzle is held stationary adjacent to the nozzle.

19. The system of claim 17, wherein the nozzle is configured to translate, and further comprising:

a wafer chuck configured to hold and rotate the wafer.

20. The system of claim 17, wherein the control system is configured to adjust a polishing current or voltage applied to the stream of electrolyte or adjust a polishing duration of the portion.

21. The system of claim 16, wherein the control system is configured to determine the adjustment to the amount that the portion is electropolished in advance of electropolishing the portion by an offset time.

22. The system of claim 16, further comprising:

a thickness metrology tool, wherein the control system obtains a map of the thickness measurement of the metal layer from the thickness metrology tool.

23. The system of claim 16, wherein the electropolishing module comprises:

an end point detector configured to measure the thickness of the metal layer.

24. The system of claim 23, wherein the electropolishing module further comprises:

a wafer chuck configured to hold, rotate, and translate the wafer while the end point detector is held stationary adjacent to the metal layer.

25. The system of claim 23, wherein the electropolishing module further comprises:

a wafer chuck configured to hold and rotate the wafer while the end point detector is translated.

26. The system of claim 23, wherein the end point detector is an optical sensor or an eddy current sensor.

27. The system of claim 23, wherein the end-point detector is configured to determine an end to polishing the portion based on a metal density of pattern on the wafer.

28. The system of claim 16, wherein the electropolishing module comprises:

a first processing chamber;

a first subsystem configured to control the first process chamber;

a second processing chamber; and

a second subsystem configured to control the second process chamber,

wherein the control system is connected to the first and second subsystems.

29. A method of polishing a metal layer formed on a semiconductor wafer, wherein the metal layer is formed on a barrier layer, which is formed on a dielectric layer having a recessed area and a non-recessed area, and wherein the metal layer covers the recessed area and the non-recessed areas of the dielectric layer, the method comprising:

polishing the metal layer to remove the metal layer covering the non-recessed area; and

polishing the metal layer in the recessed area to a height below the non-recessed area, wherein the height is equal to or greater than a thickness of the barrier layer.

30. The method of claim 29, wherein polishing the metal layer comprises electropolishing the metal layer.

31. The method of 30, wherein electropolishing the metal layer comprises:

applying a stream of electrolyte to a portion of the metal layer through a nozzle adjacent to the portion of the metal layer.

32. The method of claim 31, further comprising:

holding, rotating, and translating the wafer using a wafer chuck while the nozzle is held stationary.

33. The method of claim 31, further comprising:

holding and rotating the wafer using a wafer chuck while the nozzle is translated.

34. The method of claim 29, further comprising:

after polishing the metal layer, removing the barrier layer from the non-recessed area using plasma etching.

35. The method of claim 34, wherein plasma etching comprises using an etching gas, and wherein an additive is added to the etching gas to form a residue on the metal layer and the barrier layer in the recessed area.

36. The method of claim 34, further comprising:

removing a portion of the recessed and non-recessed area using plasma etching, wherein the etch rate of the barrier layer within the recessed area is equal to or higher than the etch rate of the dielectric layer.

37. The method of claim 29, wherein a hard mask layer is disposed between the dielectric layer and barrier layer, and wherein the height is less than the sum of the thickness of the barrier layer and a thickness of the hard mask layer.

38. The method of claim 37, wherein a sacrificial layer is disposed between the hard mask layer and barrier layer, wherein the hard mask layer has a lower removal rate than the barrier layer and the sacrificial layer has a removal rate equal to or greater than the barrier layer.

39. The method of claim 29, wherein the dielectric layer includes a low-k dielectric material, and the metal layer includes copper.

40. A layer of a semiconductor wafer comprising:

a dielectric layer having recessed and non-recessed area;

a barrier layer deposited above the dielectric layer; and

a metal layer deposited on the barrier layer, wherein the metal layer is removed from the non-recessed area of the dielectric layer and polished in the recessed area to a height below the non-recessed area, wherein the height is equal to or greater than a thickness of the barrier layer.

41. The layer of a semiconductor wafer of claim 40, further comprising:

a hard mask layer disposed between the dielectric layer and barrier layer, wherein the height is less than the sum of the thickness of the barrier layer and a thickness of the hard mask layer.

42. The layer of a semiconductor wafer of claim 41, further comprising:

a sacrificial layer disposed between the hard mask layer and barrier layer, wherein the hard mask layer has a lower removal rate than the barrier layer and the sacrificial layer has a removal rate equal to or greater than the barrier layer.

43. The layer of semiconductor wafer of claim 40, wherein the dielectric layer includes a low-k dielectric material, and the metal layer includes copper.